Homework 1

(Due date: September 15th @ 5:30 pm)
Presentation and clarity are very important!

Problem 1 (25 pts)

a) Simplify the following functions using ONLY Boolean Algebra Theorems. For each resulting simplified function, sketch the logic circuit using AND, OR, XOR, and NOT gates. (12 pts)

- ✓ $F(X,Y,Z) = \prod(M_1, M_2, M_4, M_6)$
- ✓ $F = \overline{(X \oplus \bar{Y})Z + XY\bar{Z}}$
- ✓ $F = (A + \bar{C} + \bar{D})(\bar{B} + \bar{C} + D)(A + \bar{B} + \bar{C})$
- ✓ $F = \overline{B(\bar{C} + \bar{A}) + \overline{AB}}$

b) Using ONLY Boolean Algebra Theorems, determine whether or not the following expression is valid, i.e., whether the left- and right-hand sides represent the same function: (5 pts)

$$x_1\overline{x_3} + x_2x_3 + \overline{x_2}\,\overline{x_3} = (x_1 + \overline{x_2} + x_3)(x_1 + x_2 + \overline{x_3})(\overline{x_1} + x_2 + \overline{x_3})$$

c) For the following Truth table with two outputs: (8 pts)

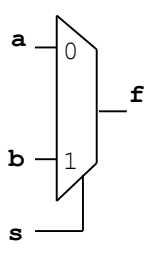
- Provide the Boolean functions using the Canonical Sum of Products (SOP), and Product of Sums (POS).
- Express the Boolean functions using the minterms and maxterms representations.
- Sketch the logic circuits as Canonical Sum of Products and Product of Sums.

x	y	z	f_1	f_2
0	0	0	0	1
0	0	1	0	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

Problem 2 (15 pts)

a) The following circuit has the following logic function: $f = \bar{s}a + sb$.

- Complete the truth table of the circuit, and sketch the logic circuit using ONLY 2-input NAND gates. (5 pts)



s	a	b	f
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

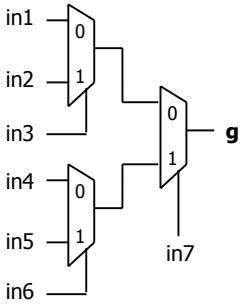
b) The circuit on the right can be used to realize various different functions. (10 pts)

- For example, the following selection of inputs produce the function: $g = x_1x_2 + x_2x_3$. Demonstrate that this is the case.

in1	in2	in3	in4	in5	in6	in7
0	x_3	x_2	0	1	x_2	x_1

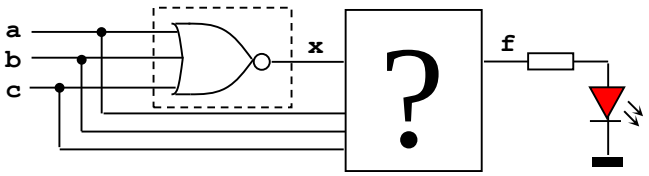
- Given the following inputs, provide the resulting function g (minimize the function).

in1	in2	in3	in4	in5	in6	in7
x_1	0	x_3	1	0	x_1	x_2



Problem 3 (12 pts)

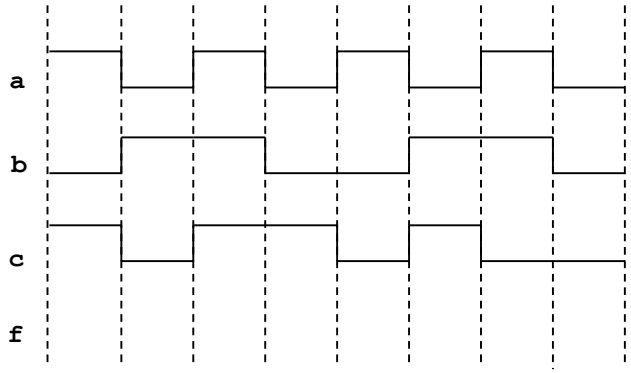
- Design a circuit (simplify your circuit) that verifies the logical operation of a 3-input NOR gate. f = '1' (LED ON) if the NOR gate does NOT work properly. Assumption: when the NOR gate is not working, it generates 1's instead of 0's and vice versa.



PROBLEM 4 (20 PTS)

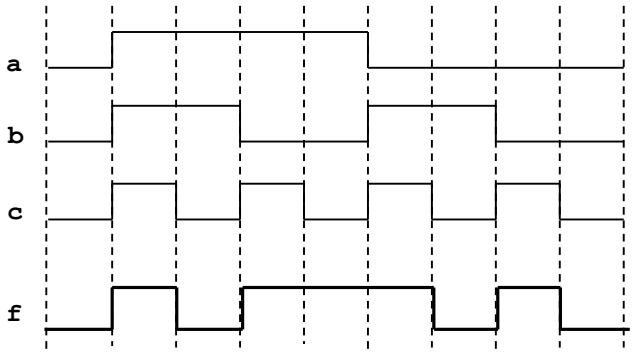
a) Complete the timing diagram of the logic circuit whose VHDL description is shown below: (6 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( a, b, c: in std_logic;
         f: out std_logic);
end circ;

architecture st of circ is
  signal x, y: std_logic;

begin
  x <= a xor b;
  y <= x nor c;
  f <= y nand (not b);
end st;
```

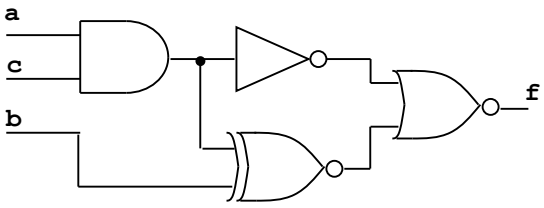


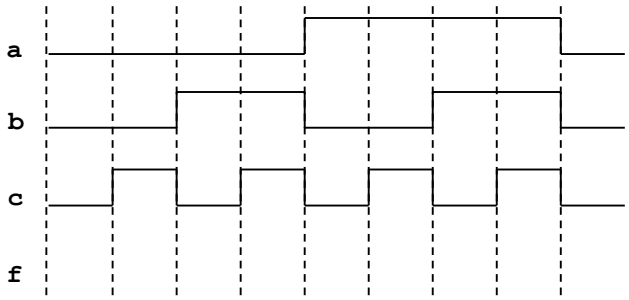
b) The following is the timing diagram of a logic circuit with 3 inputs. Sketch the logic circuit that generates this waveform. Then, complete the VHDL code. (8 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity wav is
  port ( a, b, c: in std_logic;
         f: out std_logic);
end wav;

architecture st of wav is
-- ???
begin
   -- ???
end st;
```



c) Complete the timing diagram of the following circuit: (6 pts)

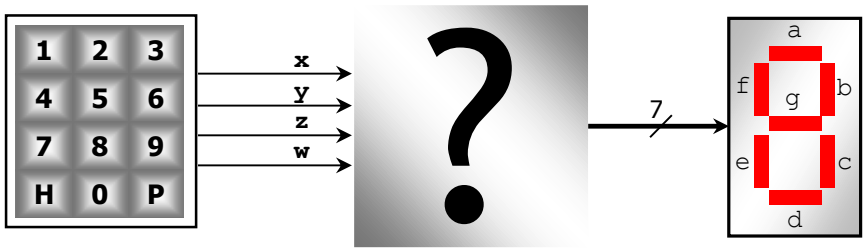




PROBLEM 5 (28 PTS)

- A numeric keypad produces a 4-bit code as shown below. We want to design a logic circuit that converts each 4-bit code to a 7-segment code, where each segment is an LED: A LED is ON if it is given a logic '1'. A LED is OFF if it is given a logic '0'.

✓ Complete the truth table for each output (a, b, c, d, e, f, g).
✓ Provide the simplified expression for each output (a, b, c, d, e, f, g). Use Karnaugh maps for c, d, e, f, g and the Quine-McCluskey algorithm for a, b. Note that it is safe to assume that the codes `1100` to `1111` will not be produced by the keypad.



Value	X	Y	Z	W	a	b	c	d	e	f	g
0	0	0	0	0							
1	0	0	0	1							
2	0	0	1	0							
3	0	0	1	1							
4	0	1	0	0							
5	0	1	0	1							
6	0	1	1	0							
7	0	1	1	1							
8	1	0	0	0							
9	1	0	0	1	1	1	1	1	0	1	1
P	1	0	1	0							
H	1	0	1	1							
	1	1	0	0							
	1	1	0	1							
	1	1	1	0							
	1	1	1	1